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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/966,316	09/27/2001	J. Daniel Mis	9180-5	5045

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EXAMINER

VESPERMAN, WILLIAM C

ART UNIT	PAPER NUMBER
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2813

DATE MAILED: 07/18/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/966,316

Applicant(s)

MIS ET AL.

Examiner

William C. Vesperman

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 03 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 27 September 2001.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-28 and 62-76 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-5,9-17,20-28 and 62-76 is/are rejected.
- 7) ☒ Claim(s) 6-8, 18 and 19 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 27 September 2001 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892) 4) ☐ Interview Summary (PTO-413) Paper No(s). _____
- 2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948) 5) ☐ Notice of Informal Patent Application (PTO-152)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2. 6) ☐ Other:

DETAILED ACTION

1. This action is in response to applicant's amendment of May 14, 2003.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claims 1, 3, 4, 5, 9, 13, 14, 15, 16, 17, 20, 24, 25, 26, 27, 28, 62, 63, 66, 68, 69, 70, 71, 72, 75 and 76 are rejected under 35 U.S.C. 103(a) as being unpatentable over Danziger et al. (US 6,221,682 B1) in view of Elenius et al. (US 2001/0011764 A1).

Danziger et al. (US 6,221,682 B1) teaches (Figures 1B - 3, columns 6, lines 45 - 36) a method of providing first and second input/output pads on the substrate in order to bond solder bumps and wire separately to individual bond pads and the bonding of die (14) to device (20) via the solder bumps.

Danziger et al. does not teach a shared metallurgy structure on the bond pads to bond solder bumps, wire or additional substrates or provide barrier layers in the range of 0.5 to 2.0 microns thick or providing a protective insulating layer on the substrate so that portions of the input/output pads are exposed.

Elenius et al. teaches (Figure 2, paragraph 0034) that the metallurgy structure comprises an under bump structure comprising of titanium formed on the bond pads,

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followed by a barrier layer of nickel vanadium and finally a passivation layer of copper formed continuously on the input and output pads deposited in continuous layers. In addition, the above structure includes a top layer of copper which the applicant has described in the detailed Description and Figure 2C as suitable for bonding wire or the bonding of solder bumps.

It would be obvious to one of ordinary skill in the art, to modify the method as taught by Danziger et al. and to include a metallurgy structure comprising of : an under bump structure comprising of a layer of titanium formed on the bond pads, followed by a barrier layer of nickel vanadium and finally a passivation layer of copper as taught by Elenius et al.

One would be motivated to modify the method as taught by Danziger et al. and incorporate a metallurgy structure consisting of an under bump structure comprising of a titanium layer formed on the bond pads, followed by a barrier layer of nickel vanadium and finally a passivation layer of copper as taught by Elenius et al. in order to achieve a structure which (1) adheres to the substrate's bond pads. and acts as a solder diffusion barrier and (2) can be applied in continuous layers in order to avoid having to deposit the same material layers repeatedly.

Elenius et al. teaches (Figure 2, page 4, paragraph 0034) that a UBM layer consisting of: titanium, nickel vanadium (barrier), copper and/or an other suitable metal such as gold is approximately 2.0 microns thick. As a result, by dividing the approximate

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total thickness of 2.0 microns by the 3 and 4 layers previously discussed, each layer or the gold layer could be approximately in the range of 0.5 to 0.67 microns thick.

The selection gold layers or the barrier layers in a range of 0.50 microns and 2.0 microns is obvious because it is a matter of determining optimum process condition by routine experimentation with a limited number of species. In re Jones, 162 USPQ 224 (CCPA 1955) (the selection of optimum ranges within prior art general conditions is obvious) and In re Boesch, 205 USPQ 215 (CCPA 1980) (discovery of optimum value of result.

Also, Elenius et al. teaches (Figure 2) providing a protective insulating layer on the substrate so that portions of the input/output pads are exposed.

One would be motivated to modify the method as taught by Danziger et al. and incorporate a protective insulating layer on the substrate so that portions of the input/output pads are exposed as taught by Elenius et al. in order to isolate the separate bond pads and insulate the substrate.

4. Claims 2, 11, 22, 67, 74 are rejected under 35 U.S.C. 103(a) as being unpatentable over Danziger et al. (US 6,221,682 B1) and Elenius et al. (US 2001/0011764 A1) as applied to Claims 1, 3, 17, 62, 69 above, and further in view of Katz et al. (US 5,234,149).

Danziger et al. and Elenius et al teaches all the limitations except do not teach that the metallurgy structure comprises a gold passivation layer on the surface opposite the input/output pads,

Katz et al. (US 5,234,149) teaches (Figure 2, column 4 - 5, lines 60 – 18)

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a shared metallurgy structure formed on the bond pads (21, 22) and capped with gold (25).

Therefore, it would be obvious to one of ordinary skill in the art, to modify the method as taught by Danziger et al. and Elenius et al. to include a metallurgy structure as taught by Katz et al. formed over the bond pads in order to bond to wire or solder bumps.

One would be motivated to modify the method as taught by Danziger et al. and Elenius et al. in order to incorporate a shared metallurgy structure formed on the bond pads (21, 22) and capped with gold (25) as taught by Katz et al. in order to reduce oxidation of the top bonding layer.

5. Claims 10,12, 21, 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Danziger et al. (US 6,221,682 B1), Elenius et al. (US 2001/0011764 A1) and Katz et al. (US 5,234,149) as applied to Claims 9, 11, 20, 22 above.

Elenius et al. teaches (Figure 2, page 4, paragraph 0034) that a UBM layer consisting of: titanium, nickel vanadium (barrier), copper and/or another suitable metal such as gold is approximately 2.0 microns thick. As a result, by dividing the approximate total thickness of 2.0 microns by the 3 and 4 layers previously discussed, each layer or the gold layer could be approximately in the range of 0.5 to 0.67 microns thick.

The selection gold layers or the barrier layers in a range of 0.50 microns and 2.0 microns is obvious because it is a matter of determining optimum process condition by

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routine experimentation with a limited number of species. In re Jones, 162 USPQ 224 (CCPA 1955) (the selection of optimum ranges within prior art general conditions is obvious) and In re Boesch, 205 USPQ 215 (CCPA 1980) (discovery of optimum value of result.

6. Claims 64, 65 and 73 are rejected under 35 U.S.C. 103(a) as being unpatentable over Danziger et al. (US 6,221,682 B1) and Elenius et al. (US 2001/0011764 A1) as applied to Claims 62, 64, 69 above.

Danziger et al. (US 6,221,682 B1) does not teach reflowing the solder structure so that the passivation layer diffuses into the solder structure and that lead from the solder structure diffuses into the first barrier layer.

Elenius et al. teaches (paragraphs 0004 –0008) that the solder bump material (containing lead) in contact with the copper passivation layer is reflowed.

Therefore, it would be obvious to one of ordinary skill in the art, to modify the method as taught by Danziger et al. and Elenius et al. to include a re-flow step as taught by Elenius et al. Since the applicant has specified in the Detailed Description stating that the passivation layer can be copper and that the barrier layer can be nickel; and that the solder contains lead as taught by Elenius et al., then it is inherent after the re-flow step, that lead from the solder structure diffuses into the passivation layer and diffuses into portions of the first barrier layer.

One would be motivated to re-flow the solder in order to improve the bond strength of the copper and nickel layers with regards to the solder layer and reduce

possible voids in the structure.

Allowable Subject Matter

7. Claims 6, 7, 8, 18 and 19 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

8. The following is a statement of reasons for the indication of allowable subject matter.

The prior art does not fairly teach or suggest that the method of providing the barrier layers comprise selectively electroplating the barrier layer on the under-bump metallurgy layer and providing the passivation layers comprise selectively electroplating the passivation layer on the barrier layer. The barrier layer comprises a nickel layer free of lead and an alloy layer including nickel and lead between the nickel layer free of lead and the solder structure.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Jao (US 6,415,974 B2) teaches a structure with solderbumps with improved coplanarity.

Chiang (US 2002/0086520) teaches a semiconductor device having a bump electrode.

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Yung (US 5,162,257) teaches a solder bump fabrication method.

Ma (US 6,208,018 B1) teaches a piggyback multiple dice assembly.

Merrill et al. (US 5,886,393) teaches a bonding wire inductor for use in an integrated circuit.

Mis (5,902,686) teaches methods for forming an inter-metallic region between a solder bump and a under-bump metallurgy region.

Kuo (US 2002/01978842 A1) teaches a solder bump process using a solder reservoir.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to William C. Vesperman whose telephone number is 703-305-1939. The examiner can normally be reached on Mon. - Fri., 8:00 - 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead, Jr. can be reached on 703-308-4940. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9318 for regular communications and 703-872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

WCV

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July 7, 2003


CARL WHITEHEAD, JR.
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800